WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a CPU core; and

a flash memory comprising at least one memory transistor, said memory transistor comprising:

a source region, a drain region and an active region formed in a semiconductor,

said active region comprising:

a plurality of impurity regions provided in a stripe shape in a channel length direction,

a plurality of intrinsic or substantially intrinsic channel forming regions interposed between the plurality of impurity regions, and

wherein the memory transistor stores multi-valued data.

2. A semiconductor device comprising:

a CPU core; and

a flash memory comprising at least one memory transistor, said memory transistor comprising:

a source region, a drain region and an active region formed in a semiconductor;

a first gate insulating film over the active region;

a plurality of floating gate electrodes;

a second gate insulating film;

a control gate electrode,

said active region comprising:

a plurality of impurity regions provided in a stripe shape in a channel length direction,

a plurality of intrinsic or substantially intrinsic channel forming regions interposed between the plurality of impurity regions,

wherein each of the plurality of floating gate electrodes is provided over each of the plurality of channel forming regions via the first gate insulating film,

wherein the control gate electrode is overlapped with the plurality of floating gate electrodes via the second gate insulating film,

wherein the memory transistor stores multi-valued data.

3. A semiconductor device comprising:

a CPU core; and

a flash memory comprising at least one memory transistor, said memory transistor comprising:

a source region, a drain region and an active region formed in a semiconductor;

a first gate insulating film over the active region;

a plurality of floating gate electrodes;

a second gate insulating film;

a control gate electrode,

said active region comprising:

a plurality of impurity regions provided in a stripe shape in a channel length direction,

a plurality of intrinsic or substantially intrinsic channel forming regions interposed between the plurality of impurity regions,

wherein each of the plurality of floating gate electrodes is provided over each of the plurality of channel forming regions via the first gate insulating film,

wherein the control gate electrode is overlapped with the plurality of floating gate electrodes via the second gate insulating film,

wherein an electric potential of each of the plurality of impurity regions is independently controlled,

wherein the memory transistor stores multi-valued data.

4. A semiconductor device according to claim 2,

wherein each of the plurality of floating gate electrodes is partially overlapped with one of the plurality of impurity regions via the first gate insulating film.

5. A semiconductor device according to claim 1,

wherein the plurality of impurity regions provided in the active region are formed continuously in at least one of the source region and the drain region.

6. A semiconductor device according to claim 1,

wherein each of the plurality of impurity regions comprises an element selected from Group 13 or Group 15 of the Periodic Table.

7. A semiconductor device according to claim 1,

wherein each of the plurality of impurity regions comprises an element selected from Group 13 or Group 15 of the Periodic Table,

wherein each of the plurality of impurity regions suppresses a depletion layer spreading from the drain region to the source region.

8. A semiconductor device according to claim 1,

wherein each of the plurality of impurity regions comprises an element at a concentration in a range of 1×10^{17} to 5×10^{20} atoms/cm^3.

9. A semiconductor device according to claim 1,

wherein a channel length of the memory transistor is in a range of 0.01 to 1 μm.

10. A semiconductor device according to claim 1,

wherein a width of each of the plurality of impurity regions is in a range of 0.01 to 1 μm.

11. A semiconductor device according to claim 1,

wherein a width of each of the plurality of channel forming regions is in a range of 0.01 to 1 μm.

12. A semiconductor device according to claim 1 wherein said semiconductor device is a microprocessor.

13. A semiconductor device according to claim 2,

wherein the plurality of impurity regions provided in the active region are formed continuously in at least one of the source region and the drain region.

14. A semiconductor device according to claim 2,

wherein each of the plurality of impurity regions comprises an element selected from Group 13 or Group 15 of the Periodic Table.

15. A semiconductor device according to claim 2,

wherein each of the plurality of impurity regions comprises an element selected from Group 13 or Group 15 of the Periodic Table,

wherein each of the plurality of impurity regions suppresses a depletion layer spreading from the drain region to the source region.

16. A semiconductor device according to claim 2,

wherein each of the plurality of impurity regions comprises an element at a concentration in a range of 1×10^{17} to 5×10^{20} atoms/cm^3.

17. A semiconductor device according to claim 2,

wherein a channel length of the memory transistor is in a range of 0.01 to 1 μm.

18. A semiconductor device according to claim 2,

wherein a width of each of the plurality of impurity regions is in a range of 0.01 to 1 μm.

19. A semiconductor device according to claim 2,

wherein a width of each of the plurality of channel forming regions is in a range of 0.01 to 1 μm.

20. A semiconductor device according to claim 2 wherein said semiconductor device is a microprocessor.

21. A semiconductor device memory according to claim 3,

wherein each of the plurality of floating gate electrodes is partially overlapped with one of the plurality of impurity regions via the first gate insulating film.

22. A semiconductor device according to claim 3,

wherein the plurality of impurity regions provided in the active region are formed continuously in at least one of the source region and the drain region.

23. A semiconductor device according to claim 3,

wherein each of the plurality of impurity regions comprises an element selected from Group 13 or Group 15 of the Periodic Table.

24. A semiconductor device according to claim 3,

wherein each of the plurality of impurity regions comprises an element selected from Group 13 or Group 15 of the Periodic Table,

wherein each of the plurality of impurity regions suppresses a depletion layer spreading from the drain region to the source region.

25. A semiconductor device according to claim 3,

wherein each of the plurality of impurity regions comprises an element at a concentration in a range of 1×10^{17} to 5×10^{20} atoms/cm^3.

26. A semiconductor device according to claim 3,

wherein a channel length of the memory transistor is in a range of 0.01 to 1 μm.

27. A semiconductor device according to claim 3,

wherein a width of each of the plurality of impurity regions is in a range of 0.01 to 1 μm.

28. A semiconductor device according to claim 3,

wherein a width of each of the plurality of channel forming regions is in a range of 0.01 to 1 μm.

29. A semiconductor device according to claim 3 wherein said semiconductor device is a microprocessor.

30. A mobile phone comprising:

a display; and

at least one memory transistor, said memory transistor comprising:

a source region, a drain region and an active region formed in a semiconductor,

said active region comprising:

a plurality of impurity regions provided in a stripe shape in a channel length direction,

a plurality of intrinsic or substantially intrinsic channel forming regions interposed between the plurality of impurity regions, and

wherein the memory transistor stores multi-valued data.

31. A mobile phone comprising:

a display; and

at least one memory transistor, said memory transistor comprising:

a source region, a drain region and an active region formed in a semiconductor;

a first gate insulating film over the active region;

a plurality of floating gate electrodes;

a second gate insulating film;

a control gate electrode,

said active region comprising:

a plurality of impurity regions provided in a stripe shape in a channel length direction,

a plurality of intrinsic or substantially intrinsic channel forming regions interposed between the plurality of impurity regions,

wherein each of the plurality of floating gate electrodes is provided over each of the plurality of channel forming regions via the first gate insulating film,

wherein the control gate electrode is overlapped with the plurality of floating gate electrodes via the second gate insulating film,

wherein the memory transistor stores multi-valued data.

32. A mobile phone comprising:

a display; and

at least one memory transistor, said memory transistor comprising:

a source region, a drain region and an active region formed in a semiconductor;

a first gate insulating film over the active region;

a plurality of floating gate electrodes;

a second gate insulating film;

a control gate electrode,

said active region comprising:

a plurality of impurity regions provided in a stripe shape in a channel length direction,

a plurality of intrinsic or substantially intrinsic channel forming regions interposed between the plurality of impurity regions,

wherein each of the plurality of floating gate electrodes is provided over each of the plurality of channel forming regions via the first gate insulating film,

wherein the control gate electrode is overlapped with the plurality of floating gate electrodes via the second gate insulating film,

wherein an electric potential of each of the plurality of impurity regions is independently controlled,

wherein the memory transistor stores multi-valued data.

33. A mobile phone according to claim 32,

wherein each of the plurality of floating gate electrodes is partially overlapped with one of the plurality of impurity regions via the first gate insulating film.